A) The Applicable Law

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131.

B) The References

Manning (U. S. Patent No. 5,610,864): teaches a memory device which may be accessed using latched row and column addresses. (Col. 4, lines 10-28). The device may also be accessed using a high-speed burst mode of operation, wherein the address is incremented internal to the device, using transitions of the column address select (/CAS) signal, following the assertion of a single external column address. (Col. 4, lines 29-49). Switching between the burst extended data out (EDO) mode and the standard EDO mode is described. (Col. 6, lines 14-22). Switching between interleaved and linear addressing modes is mentioned. (Col. 6, lines 30-34). The possibility of applying a pipelined architecture to Manning's invention is also mentioned. (Col. 5, lines 43-46). Operation of the pipelined architecture is said to be characterized by having a memory throughput of less than one access per cycle, such that the data coming out of the device is offset by some number of cycles equal to the pipeline length. (Col. 5, lines 46-50).

C.1) The Rejection Under § 112:

Claim 61 was rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled

in the art that the inventor, at the time the application was filed, had possession of the claimed invention. Because the elements of claim 61 were indeed described in the application at the time of filing, the Applicants respectfully traverse this rejection.

The assertion was made "that 'selecting a pipelined mode of operation; proving [sic] a new external address for every [sic] associated with — while in a burst mode of operation; providing an initial external address associated — in the pipelined mode of operation; and while in the burst mode of operation, generating at lest [sic] one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation' was not described in the specification." However, each of these elements is in fact described in several places in the application.

For example "selecting a pipelined mode of operation" is taught at pg. 29, lines 1, and 8-9, among numerous others. "Providing a new external address for every access associated with asynchronously accessing the ... device while in a burst mode of operation" is discussed at pg. 35, lines 8-10 and pg. 36, lines 9-10. "Switching modes to a burst mode of operation" is disclosed at pg. 30, lines 1-3 and 24-25, among numerous others. "Providing an initial external address associated with asynchronously accessing the ... device in the pipelined mode of operation" is noted at FIG. 15, time 210 and pg. 36, lines 14-15. Finally, "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation" is shown at pg. 27, lines 1-11; pg. 38, lines 11-15; and pg. 39, lines 9-16. Thus, since each of the elements of claim 61 were indeed disclosed in the application at the time of filing, it is respectfully requested that the rejection under 35 USC § 112, first paragraph, be reconsidered and withdrawn.

C.2) The Rejection Under § 102:

Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 were rejected under 35 USC § 102(e) as being anticipated by Manning. First, the Applicants do not admit that Manning is prior art and reserve the right to swear behind this reference in the future. Second, the Applicants respectfully submit that a case of anticipation under 35 U.S.C. § 102(e) has not been established because Manning does not disclose each and every element of claims 1-9, 33-35, 46, 48-50, 59-61, and

63-64. Therefore, the Applicants respectfully traverse this rejection under 35 USC § 102(e).

Why the reference does not disclose each and every element of the claimed subject matter as arranged in the claims.

Manning specifically fails to disclose "circuitry ... configured to switch between the pipelined mode and the burst mode" as claimed by the Applicants in claim 1. Similarly, Manning fails to disclose that the burst mode and the pipelined mode are "extended data out modes" (claims 2-4); or that the "pipelined/burst mode circuitry" includes: a "buffer for storing an (external) address", a "counter for incrementing an address", "is coupled for receiving an external address", or"multiplexed devices for providing an internally generated address" (claims 5-9).

Further, Manning does not teach "selecting between" a "burst mode ... and" a "pipelined mode", or switching between such modes (claims 33-34, 46, 59-61); much less how addresses are supplied while selecting or switching modes (claim 35), or what type of switching environment may be used in burst and pipelined modes of operation (claims 48-49). Finally, Manning does not describe a system including a microprocessor and memory "selectively operable either in a burst mode or a pipelined mode", or a storage device/memory including circuitry "switchable between burst and pipeline modes of operation" (claims 50, and 63-64).

Several assertions were made which attribute support to various concepts allegedly disclosed by Manning in the Office Action mailed to the Applicants on 3/15/02 (Paper 31, pages 7-9). However, a careful reading of each citation reveals that the discussion of the asserted elements is either vague, nonexistent, or, in at least one case, completely in error. These assertions have been made with respect to:

Claims 2, 3 - Manning does not disclose that the pipelined mode is an EDO mode of operation (the two concepts are never discussed in conjunction with each other).

Claim 9 - Manning does not disclose mode selection circuitry which includes a multiplexed device (the components referenced in the Office Action are an address counter 26 and a column address decoder 30).

Claim 34 - Manning does not disclose *switching* between the pipelined mode and the burst mode (Manning merely refers to the possibility of using a pipelined *architecture*).

Claim 35 - Manning does not disclose selecting an external address along with *selecting* between a burst mode and a pipelined mode (since Manning never discloses selecting between burst and pipelined modes in the same device).

Claims 48, 49 - Manning does not disclose several switching environments in conjunction with burst and pipelined modes (Manning merely refers to the possibility of using a pipelined *architecture*).

Two more erroneous assertions are directed toward all pending claims. First, it is not true that one must"select pipeline mode" to "work in the pipeline architecture" (See Paper 31, page 11 - if a device always operates in the pipelined mode, the pipelined mode does not have to be selected). Second, in contrast to assertions tendered by the Office, the feature of switching between pipelined and burst mode operations in the same memory are included in each of the rejected claims, since each claim is directed toward a single device, accessing a single device, accessing different locations in a single device, or a single device included in a system.

Why the reference does not disclose the claimed subject matter in as complete detail as is contained in the claim.

First, it should be noted that the Office has admitted that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in an Office Action mailed to the Applicants on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter. If Manning does not disclose these elements, how (specifically) does Manning support *switching* or *selecting* between burst and pipelined modes of operation, as claimed in claims 1, 33, 34, 46, 50, 59, 60, 61, 63, and 64 (and in all claims that depend from them)?

Second, the Office has failed to produce a *prima facie* case of anticipation. While the assertion is made that Manning discloses "mode circuitry to select between a burst mode and a pipelined mode", and that the circuitry is "configurable to select between [the] two modes", the Applicants' representative, after a careful study of Manning, was unable to locate any such selection circuitry, nor any aspect of such circuitry which was configurable to select between burst and pipelined modes of operation.

For example, the only references offered by the Office to support the assertion that Manning "discloses the invention as claimed" with respect to claim 1 are: Fig.1, Ref. 40; col. 5, lines 41-50; col. 6, lines 14-34; and col 7, lines 43-54. Fig. 1, Ref. 40 is a block "mode register", with no indication regarding exactly which modes may be operative, or how they may be selected. Col. 5, lines 41-50 discuss the possibility of using a pipelined architecture (e.g., perhaps this refers to a pipelined *output* stage of a burst EDO device?), but not as enabling switching between true pipeline mode or burst mode access operations, as disclosed and claimed by the Applicants. Col. 6, lines 14-34 merely describe burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Finally, col. 7, lines 43-54 speak to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Thus, Manning never discusses the ability to *select* or *switch* between burst and pipelined modes of operation, as claimed by the Applicants in independent claim 1, as well as in independent claims 33, 46, 50, 59-61, 63, and 64, and all of the claims which depend from them.

Third, the Applicants respectfully draw attention to a statement in an Office Action mailed to the Applicants on March 15, 2002 (with regard to the instant application, Paper 31, page 6) that claim 1 reads on "switching between standard fast page mode (non-EDO) and burst mode". The Applicants' representative was unable to find any portion of Manning to support the idea that the fast page mode of operation is the same as a pipelined mode of operation, and no support has been provided by the Office in response to repeated requests by the Applicants that such support for this proposition in Manning be designated with specificity.

Fourth, as mentioned in several previous responses to Office Actions in this matter, the Applicants' representative cannot find where Manning discusses that the fast page and pipelined modes are interchangeable, or combinable, such that the term "fast page pipeline" coined in several Office Actions is defined. The Applicants still fail to understand the meaning of this particular phrase, and have received no response from the Office with regard to repeated requests for a more detailed explanation. Given the lack of support for such a term, the assertion by the Office that "Manning discloses mode circuitry to select between fast page pipeline and burst; and circuitry operable in either the burst mode or the pipelined mode coupled to the mode selection circuitry and configured to select between the two modes" is simply not supported by any of the

teachings of Manning.

In short, what is discussed by Manning is not identical to the subject matter of various embodiments of the invention as required by the M.P.E.P., and therefore, the rejection is under § 102 is improper. Reconsideration and allowance of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 is respectfully requested.

C.3) Why The Claims Are Separately Patentable:

Independent claim 1 includes "circuitry ... configured to switch between the pipelined mode and the burst mode". Dependent claims 2-4 refine this concept by including the limitations of the burst mode and the pipelined mode being "extended data out modes". Dependent claims 5-9 add the limitations of having the "pipelined/burst mode circuitry" include: a "buffer for storing an (external) address" (claims 5, 8); a "counter for incrementing an address" (claim 6); coupling for receiving an external address" (claim 7); and "multiplexed devices for providing an internally generated address" (claim 9). None of these limitations depends on the other, and each dependent claim is separately patentable from the other, and from independent claim 1.

Independent method claims 33, 46, and 59-61 include the elements of "selecting between" a "burst mode ... and" a "pipelined mode", or switching between such modes, as does dependent claim 34 (which speaks to a combination of these operations). Dependent claim 35 includes a further limitation with respect to how an address may be provided during mode switching activity. Dependent claims 48-49 include limitations describing the type of switching environments that may be used during burst and pipelined modes of operation, respectively. None of these limitations depends on the other, and each dependent claim is separately patentable from the other, and from the respective independent claims.

Independent system claim 50 is directed toward a microprocessor and memory "selectively operable either in a burst mode or a pipelined mode". Independent claims 63 and 64 describe a storage device/memory including circuitry "switchable between burst and pipeline modes of operation", with the device of claim 63 including mode circuitry for "receiving a burst/pipeline signal". None of these limitations depends on the other, and each independent claim is separately patentable from the other.

C.4) Double patenting rejection:

Claims 59 and 60 were provisionally rejected under the judicially created doctrine of double patenting over claim 36 of co-pending Application No. 08/984,563. Claim 61 was provisionally rejected under the judicially created doctrine of double patenting over claim 59 of co-pending Application No. 08/984,561.

Co-pending U.S. Patent Application Serial Nos. 08/984,563 and 08/984,561 have not yet received any final indication of allowed claims. The Applicants request that the claims of the instant patent application be allowed to issue without a Terminal Disclaimer, and that the issued claims of the instant application be compared to the claims of the cited co-pending applications to determine if a judicially-created non-statutory double patenting rejection is required. If so, the Applicants will submit a Terminal Disclaimer to obviate any remaining double patenting rejections upon closing prosecution on the merits for the co-pending applications, as needed, or in the alternative, upon receiving an indication of allowance for the relevant claims in the instant application.

CONCLUSION

It is respectfully submitted that (a) all elements of claim 61 were indeed disclosed in the application, as filed, and (b) the art cited does not anticipate the claimed invention. Therefore, reconsideration and withdrawal of the rejections of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 is respectfully requested.

The Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Applicants' attorney, **Mark Muller at (210) 308-5677**, or the undersigned attorney, to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box AF, Commissioner of Patents, Washington, D.C. 20231, on this 13 day of September, 2002.

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Name

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Signature